WHAT IS CLAIMED IS:

1. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of setting the parameter includes a program operation, in which electrons are

injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the bit line,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation being shorter than that of the first programming operation.

2. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 1,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

3. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 1,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

4. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 1,

wherein each said verifying operation verifies whether the parameter of the one non-volatile multi-level memory cell has been set to the one state selected from the plurality of states, and includes comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

5. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 1,

wherein the operation of setting the parameter includes an erasure operation in which non-volatile multi-

level memory cells of one of a byte, a block and a chip level can be erased.

6. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 1,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of a non-selected cell.

7. An electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, the electrically alterable non-volatile multi-level memory device having the following operations:

an operation of controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one

state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

an operation of reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of controlling the electrical value includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the bit line,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation being shorter than that of the first programming operation.

8. The electrically alterable non-volatile multi-level memory device according to claim 7,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

9. The electrically alterable non-volatile multi-level memory device according to claim 7,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

10. The electrically alterable non-volatile multi-level memory device according to claim 7,

wherein each said verifying operation verifies whether the electrical value of the one non-volatile multi-level memory cell has been controlled to the one state selected from the plurality of states, and includes comparing the electrical value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference

parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

11. The electrically alterable non-volatile multi-level memory device according to claim 7,

wherein the operation of controlling the electrical value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

12. The electrically alterable non-volatile multi-level memory device according to claim 7,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of a non-selected cell.

13. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a control gate,

a floating gate and a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of setting the parameter includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the control gate of a memory cell to be programmed,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation being shorter than that of the first programming operation.

14. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 13,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

15. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 13,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the

second programming operation is carried out using the programming voltage of a mono-pulse.

16. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 13,

wherein each said verifying operation verifies whether the parameter of the one non-volatile multi-level memory cell has been set to the one state selected from the plurality of states, and includes comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

17. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 13,

wherein the operation of setting the parameter includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

18. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 13,

wherein a bit line coupled with a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a bit line coupled with a non-selected cell.

19. An electrically alterable non-volatile multi-level memory device including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, the electrically alterable non-volatile multi-level memory device having the following operations:

an operation of controlling an electrical value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

an operation of reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of controlling the electrical value includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to a control gate of a memory cell to be programmed,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation being shorter than that of the first programming operation.

20. The electrically alterable non-volatile multi-level memory device according to claim 19,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the

second programming operation is carried out using the programming voltage of a single pulse.

21. The electrically alterable non-volatile multi-level memory device according to claim 19,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

22. The electrically alterable non-volatile multi-level memory device according to claim 19,

wherein each said verifying operation verifies whether the electrical value of the one non-volatile multi-level memory cell has been controlled to the one state selected from the plurality of states, and includes comparing the electrical value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

23. The electrically alterable non-volatile multi-level memory device according to claim 19,

wherein the operation of controlling the electrical value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

24. The electrically alterable non-volatile multi-level memory device according to claim 19,

wherein the bit line coupled with a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a bit line coupled with a non-selected cell.

25. For an electrically alterable non-volatile multi-level memory including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, a method of operating the electrically alterable non-volatile multi-level memory, comprising:

setting a voltage threshold value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of setting the voltage threshold value of the one non-volatile multi-level memory cell includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the bit line,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first voltage threshold value change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second voltage threshold value change of the one non-volatile multi-level memory cell caused by the second programming operation.

26. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein said parameter includes a duration of the respective programming operation.

27. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the

second programming operation is carried out using the programming voltage of a single pulse.

28. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

29. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein each said verifying operation verifies whether the voltage threshold value of the one non-volatile multi-level memory cell has been set to the one state selected from the plurality of states, and includes comparing the voltage threshold value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third

verifying reference parameter and a fourth verifying reference parameter.

30. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein the operation of setting the voltage threshold value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

31. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of non-selected cell.

32. An electrically alterable non-volatile multi-level memory including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells

including a floating gate FET having a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, the electrically alterable non-volatile multi-level memory having the following operations:

an operation of controlling a voltage threshold value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

an operation of reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of controlling the voltage threshold value of the one non-volatile multi-level memory cell includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the bit line,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first voltage threshold value change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second voltage threshold value change of the one non-volatile multi-level memory cell caused by the second programming operation.

33. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein said parameter includes a duration of the respective programming operation.

34. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

35. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

36. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein each said verifying operation verifies whether the voltage threshold value of the one non-volatile multi-level memory cell has been controlled to the one state selected from the plurality of states, and includes comparing the voltage threshold value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first

verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

37. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein the operation of controlling the voltage threshold value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

38. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of a non-selected cell.

39. For an electrically alterable non-volatile multi-level memory including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a control gate, a

floating gate and a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, a method of operating the electrically alterable non-volatile multi-level memory, comprising:

setting a voltage threshold value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi- level memory cell, and

reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of setting the voltage threshold value of the one non-volatile multi-level memory cell includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the control gate of the one memory cell,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first voltage threshold value change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second voltage threshold value change of the one non-volatile multi-level memory cell caused by the second programming operation.

40. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein said parameter includes a duration of the respective programming operation.

41. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

42. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

43. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein each said verifying operation verifies whether the voltage threshold value of the one non-volatile multi-level memory cell has being set to the one state selected from the plurality of states, and includes comparing the

voltage threshold value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

44. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein the operation of setting the voltage threshold value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

45. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein a bit line coupled with a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a bit line coupled with a non-selected cell.

46. An electrically alterable non-volatile multi-level memory including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a control gate, a floating gate and a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, the electrically alterable non-volatile multi-level memory having the following operations:

an operation of controlling a voltage threshold value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

an operation of reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of controlling the voltage threshold value of the one non-volatile multi-level memory cell includes a program operation, in which electrons are

injected into the floating gate of the one non-volatile multi-level memory cell using at least one programming voltage applied to the control gate of the one memory cell,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first voltage threshold value change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second voltage threshold value change of the one non-volatile multi-level memory cell caused by the second programming operation.

47. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein said parameter includes a duration of the respective programming operation.

48. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

49. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

50. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein each said verifying operation verifies whether the voltage threshold value of the one non-volatile multi-level memory cell has been controlled to the one state selected from the plurality of states, and includes

comparing the voltage threshold value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

51. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein the operation of controlling the voltage threshold value includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

52. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein a bit line coupled with a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a bit line coupled with a non-selected cell.

53. For an electrically alterable non-volatile multi-level memory device including a plurality of non-volatile

multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a control gate, a floating gate and a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, a method of operating the electrically alterable non-volatile multi-level memory device, comprising:

setting a parameter of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of setting the parameter includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using programming voltages applied to the bit line and the control gate, respectively,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation being shorter than that of the first programming operation.

54. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 53,

wherein the first programming operation is carried out using the programming voltages, each of which is of a single pulse, and the second programming operation is carried out using the programming voltages, each of which is of a single pulse.

55. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 53,

wherein the first programming operation is carried out using the programming voltages, each of which is of a mono-

pulse, and the second programming operation is carried out using the programming voltages, each of which is of a mono-pulse.

56. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 53,

wherein each said verifying operation verifies whether the parameter of the one non-volatile multi-level memory cell has been set to the one state selected from the plurality of states, and includes comparing the parameter of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

57. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 53,

wherein the operation of setting the parameter includes an erasure operation in which non-volatile multi-

level memory cells of one of a byte, a block and a chip level can be erased.

58. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 53,

wherein the control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of a non-selected cell.

59. An electrically alterable non-volatile multi-level memory including a plurality of non-volatile multi-level memory cells, each of the multi-level memory cells including a floating gate FET having a control gate, a floating gate and a channel with electrically alterable voltage threshold value, electrons being capable of being injected into the floating gate, the electrically alterable non-volatile multi-level memory having the following operations:

an operation of controlling a voltage threshold value of at least one non-volatile multi-level memory cell of the plurality of non-volatile multi-level memory cells to one

state selected from a plurality of states including at least a first state, a second state, a third state and a fourth state in response to information to be stored in the one non-volatile multi-level memory cell, and

an operation of reading status of the one non-volatile multi-level memory cell from an output from a bit line coupled to a drain terminal of the one non-volatile multi-level memory cell,

wherein the operation of controlling the voltage threshold value of the one non-volatile multi-level memory cell includes a program operation, in which electrons are injected into the floating gate of the one non-volatile multi-level memory cell using programming voltages applied to the bit line and the control gate, respectively,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations include a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined

value different from the first predetermined value so that a first voltage threshold value change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second voltage threshold value change of the one non-volatile multi-level memory cell caused by the second programming operation.

60. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein said parameter includes a duration of the respective programming operation.

61. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein the first programming operation is carried out using the programming voltages, each of which is of a single pulse, and the second programming operation is carried out using the programming voltages, each of which is of a single pulse.

62. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein the first programming operation is carried out using the programming voltages, each of which is of a mono-pulse, and the second programming operation is carried out using the programming voltages, each of which is of a mono-pulse.

63. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein each said verifying operation verifies whether the voltage threshold value of the one non-volatile multi-level memory cell has been controlled to the one state selected from the plurality of states, and includes comparing the voltage threshold value of the one non-volatile multi-level memory cell with one of a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter.

64. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein the operation of controlling the voltage threshold value includes an erasure operation in which non-

volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

65. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein a bit line coupled with a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a bit line coupled with a non-selected cell.

66. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 1,

wherein the program operation includes a verify operation before the series of programming operations.

67. The electrically alterable non-volatile multi-level memory device according to claim 7,

wherein the program operation includes a verify operation before the series of programming operations.

68. The method of operating the electrically alterable non-volatile multi-level memory device according to claim 13,

wherein the program operation includes a verify operation before the series of programming operations.

69. The electrically alterable non-volatile multi-level memory device according to claim 19,

wherein the program operation includes a verify operation before the series of programming operations.

70. The method of operating the electrically alterable non-volatile multi-level memory according to claim 25,

wherein the program operation includes a verify operation before the series of programming operations.

71. The electrically alterable non-volatile multi-level memory according to claim 32,

wherein the program operation includes a verify operation followed by the series of programming operations.

72. The method of operating the electrically alterable non-volatile multi-level memory according to claim 39,

wherein the program operation includes a verify operation followed by the series of programming operations.

73. The electrically alterable non-volatile multi-level memory according to claim 46,

wherein the program operation includes a verify operation followed by the series of programming operations.

74. The method of operating the electrically alterable non-volatile multi-level memory according to claim 53,

wherein the program operation includes a verify operation followed by the series of programming operations.

75. The electrically alterable non-volatile multi-level memory according to claim 59,

wherein the program operation includes a verify operation followed by the series of programming operations.